R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

CLAIM REJECTIONS UNDER 35 U.S.C. §112

The rejection of claims 1-11, 21, 22, 25 and 26 under 35 U.S.C. §112, first paragraph, is respectfully traversed and should be withdrawn.

The Office Action fails to provide evidence or reasoning why one of ordinary skill in the art would be unable to make and/or use the invention. MPEP §2164.04 states:

> In order to make a rejection, the examiner has the initial burden to establish a reasonable basis to question the enablement provided for the claimed invention. *In re Wright*, 999 F.2d 1557, 1562, 27 USPQ2d 1510, 1513 (Fed. Cir. 1990). ... [T]he examiner should specifically identify what information is missing and **why** one skilled in the art could not supply the information without undue experimentation. ... However, **specific technical reasons are always required.** (Emphasis added)

The assertion on page 3 of the Office Action that undue experimentation would be necessary appears to be merely a conclusory statement lacking the required support. Therefore, the initial burden for the 35 U.S.C. §112 rejection has not been meet. As such, the Examiner is respectfully requested to either (i) provide evidence and/or reasoning why one of ordinary skill in the art would be unable to practice the invention or (ii) withdraw the rejection.

CLAIM INTERPRETATION

The interpretation that "adding a digital signature to an analog signal" is similar to "generating a digital signal proportional to average supply current" is respectfully traversed and should be withdrawn.

The Office Action fails to interpret the claims both (i) consistent with the specification and (ii) consistent with those of ordinary skill in the art. MPEP §2111 states:

> During patent examiner, the pending claims must be "given their broadest reasonable interpretation **consistent with the specification.**" *In re Hyatt*, 211 F.3d 1367, 1372, 54 USPQ2d 1664m 1667 (Fed. Cir. 2000) . . . The broadest reasonable interpretation of the claims must also be **consistent with the interpretation that those skilled in the art would reach**. *In re Cortright*, 165 F.3d 1353, 1359, 48 USPQ2d 1464, 1468 (Fed. Cir. 1999). (Emphasis added)

The Office Action provides no evidence or convincing line of reasoning that "generating a digital signature proportional to average supply current" is consistent with the specification and would be reached by one of ordinary skill in the art. Therefore, the interpretation on page 4 of the Office Action appear to be merely a conclusory statement lacking support. Furthermore, MPEP §2111.01 states:

> During examination, the claims must be interpreted as broadly as their terms reasonably allow. ... This means that the words of the claim must be given their plain meaning unless applicant has provided a clear definition in the specification. ... The broadest reasonable interpretation of the claims must be consistent with the interpretation that those skilled in the art would reach.

The claim interpretation provided in the Office Action appears to go well beyond the plain meaning of the claim language by completely eliminating the "adding" step. As such, the Examiner is respectfully requested to either (i) provide evidence and/or a convincing line of reasoning why the asserted interpretation is both consistent with the specification and consistent with one of ordinary skill in the art or (ii) withdraw the interpretation.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-11 and 21-29 under 35 U.S.C. §102(b) as being anticipated by publication "A Current Integrator for BIST of Mixed-Signals IC's" by Tabatabaei et al. (hereafter Tabatabaei) is respectfully traversed and should be withdrawn.

Tabatabaei concerns a current integrator for BIST of mixed-signal ICs (Title).

Claim 1 provides (in part) a step for generating one or more source signals by adding a digital signature to each of one or more analog signals. In contrast, Tabatabaei appears to be silent regarding adding digital signatures to analog signals. Furthermore, Tabatabaei does not appear discuss adding a signal "n-bit N" (asserted similar to the claimed digital signature) to a signal Idd (asserted similar to the claimed analog signal) or any other analog signal. Therefore, Tabatabaei does not appear to disclose or suggest a step for generating one or more source signals by adding a digital signature to each of one or more analog signals as presently claimed. Claim 9 provides language similar to

claim 1. As such, the claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 1 further provides a step for modeling an analog design using source signals having digital signatures in place of analog signals for verifying connectivity. Despite the assertion on page 4 of the Office Action, the first paragraph in section 3 of Tabatabaei appears to be silent regarding both (i) modeling an analog design using source signals having digital signatures **in place of** analog signals and (ii) verifying connectivity. Therefore, Tabatabaei does not appear to disclose or suggest a step for modeling an analog design using source signals having digital signatures in place of analog signals for verifying connectivity as presently claimed.

Assuming, *arguendo*, that the interpretation on page 4 of the Office Action is correct (for which Applicants' representative does not agree), the Office Action fails to establish that Tabatabaei discusses modeling a circuit with the signal "n-bit N" in place of analog signals as presently claimed. Therefore, *prima facie* anticipation has not been established. As such, the Examiner is respectfully requested to either (i) clearly and concisely identify where Tabatabaei discusses both (a) substituting source signals in place of analog signals and (b) verifying connectivity or (ii) withdrawn the rejection.

Claim 9 further provides a step for verifying connectivity of an attributed signals from a source block to a

destination block within a model of an analog device by verifying reception of unique digital signatures associated with each of the attributed signals at the destination block. In contrast, Tabatabaei appears to be silent regarding both (i) verification of connectivity between blocks and (ii) verification for reception of digital signatures at a destination block. Therefore, Tabatabaei does not appear to disclose or suggest a step for verifying connectivity of an attributed signals from a source block to a destination block within a model of an analog device by verifying reception of unique digital signatures associated with each of the attributed signals at the destination block as presently claimed. As such, claim 9 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 23 provides a source for a plurality of signals and a simulator connected to the source. Despite the assertion on page 6 of the Office Action, Tabatabaei appears to be silent regarding a source for signals and a simulator connected to the source as presently claimed. Therefore, *prima facie* anticipation of the claimed structure has not been established.

Claim 23 further provides that the simulator is configured to verify a connectivity of an analog signal in an analog design using a digital signature. Despite the assertion on page 6 of the Office Action, Tabatabaei appears to be silent regarding a simulator verifying connectivity of an analog signal in an analog design using a digital signature as presently claimed.

As claim 23 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 3 provides that each digital signature corresponds to a type of the analog signals having a predetermined parameter. Despite the assertion on page 5 of the Office Action, the Abstract of Tabatabaei appears to be silent regarding both (i) types of analog signals and (ii) predetermined parameters of the analog signals. Therefore, Tabatabaei does not appear to disclose or suggest that each digital signature corresponds to a type of the analog signals having a predetermined parameter as presently claimed. As such, the Examiner is respectfully requested to either (i) clearly and concisely identify both the types of analog signals and the associated predetermined parameters allegedly disclosed by Tabatabaei or (ii) withdraw the rejection.

Claim 4 provides that each of the digital signatures comprises a unique pulse width. Despite the assertion on page 5 of the Office Action, Tabatabaei appears to be silent regarding the signal "n-bit N" having unique pulse widths as presently claimed. Claim 28 provides language similar to claim 4. As such, the Examiner is respectfully requested to either (i) provide clear and concise evidence where the Tabatabaei allegedly discloses digital signatures having unique pulse widths or (ii) withdraw the rejections of claims 4 and 28.

Claim 5 provides a step for performing verification of an analog design. Despite the assertion on page 5 of the Office Action, the first paragraph of section 3 in Tabatabaei appears to

be silent regarding circuit verification as presently claimed. As such, the Examiner is respectfully requested to either (i) quote the language of Tabatabaei allegedly discussing verification or (ii) withdraw the rejection.

Claim 6 provides a step for verifying a connectivity of analog signals through an analog design. Despite the assertion on page 5 of the Office Action, the first paragraph of section 3 in Tabatabaei appears to be silent regarding verifying connectivity for an analog signal as presently claimed. As such, the Examiner is respectfully requested to either (i) quote the language of Tabatabaei allegedly discussing verifying connectivity of an analog signal or (ii) withdraw the rejection.

Claim 7 provides a step for verifying a model of an analog block within an analog design configured to receive at least a particular one of the analog signals. Despite the assertion on page 5 of the Office Action, Tabatabaei appears to be silent regarding a model of an analog block receiving a signal SIN2 (asserted similar to the claimed at least one particular analog signal). Furthermore, Tabatabaei appears to be silent regarding adding a digital signature to the signal SIN2 from step (A) of base claim 1. Therefore, Tabatabaei does not appear to disclose or suggest a step for verifying a model of an analog block within an analog design configured to receive at least a particular one of the analog signals as presently claimed. As such, the Examiner is respectfully requested to either (i) (a) identify the model of an analog block with an analog circuit discussed by Tabatabaei

allegedly similar to the claimed model and (b) provide clear and concise evidence where a digital signature is added to the signal SIN2 of Tabatabaei or (ii) withdraw the rejection.

Claim 8 provides a step for verifying an output signal of the analog block (from claim 7) for the digital signature associated with the particular one of the analog signals. In contrast, the Office Action appears to be asserting on page 5 that the signal SIN2 is both the input and output of some unidentified analog block. Since the signal SIN2 cannot simultaneously anticipate two different claimed signals, *prima facie* anticipation has not been established. As such, claim 8 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 10 provides a step of disabling processing of a particular one of an plurality of attributed signals if a particular signal is not verified at a destination block. Despite the assertion on page 6 of the Office Action, the first paragraph in section 3 of Tabatabaei appears to be silent regarding disabling processing of a particular one of an plurality of attributed signals if a particular signal is not verified at a destination block as presently claimed. Therefore, the Examiner is respectfully requested to either (i) clearly show how the language of Tabatabaei allegedly anticipating the claimed step is being applied to the claim or (ii) withdraw the rejection.

Claim 11 provides a step for verifying a model of a destination block configured to receive at least one of a plurality of attributed signals. Despite the assertion on page 6 of the

Office Action, Tabatabaei appears to be silent regarding verifying a model of a destination block configured to receive at least one of a plurality of attributed signals as presently claimed. As such, the Examiner is respectfully requested to either (i) (a) clearly identify the model of a destination block allegedly discussed by Tabatabaei and (b) clearly identify the signal of Tabatabaei allegedly similar to the claimed at least one of a plurality of attributed signals or (ii) withdraw the rejection.

Claim 21 provides that each of the digital signatures comprise a plurality of pulses. Despite the assertion on page 6 of the Office Action, Tabatabaei appears to be silent regarding the signal "n-bit N" comprising a plurality of pulses. Claim 27 provides language similar to claim 21. As such, the Examiner is respectfully requested to either (i) provide clear and concise evidence where Tabatabaei allegedly describes the signal "n-bit N" has comprising a plurality of pulses of (ii) withdraw the rejections of claims 21 and 27.

Claim 22 provides that each of the digital signatures comprise a varying frequency signal. Despite the assertion on page 6 of the Office Action, the first paragraph of section 3 in Tabatabaei appears to be silent regarding the signal "n-bit N" (asserted similar to the claimed digital signal) comprising a varying frequency signal. Claim 29 provides language similar to claim 22. Therefore, the Examiner is respectfully requested to either (i) provide clear and concise evidence where Tabatabaei allegedly discloses the signal "n-bit N" comprising a varying

frequency signal or (ii) withdraw the rejections of claims 22 and 29.

Claim 24 provides that a source for a plurality of signals (connected to a simulator) comprises an analog source block. Despite the assertion on page 7 of the Office Action, Tabatabaei appears to be silent regarding a block CUT (source of the signal Idd - asserted similar to one of the claimed analog signals) being a source for a plurality of signals. Therefore, Tabatabaei does not appear to disclose or suggest that a source for a plurality of signals comprises an analog source block as presently claimed.

Furthermore, Tabatabaei appears to be silent regarding the block CUT being connected to a simulator as presently claimed. Therefore, *prima facie* anticipation has not been established.

Furthermore, Tabatabaei appears to be silent regarding the block CUT being an analog source block. Therefore, *prima facie* anticipation has not been established. As such, claim 24 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 25 provides that the source block comprises an adder block. Despite the assertion on page 7 of the Office Action, Tabatabaei appears to be silent that a circuit Built-In Current Monitor (BICM) is similar to an adder block. Therefore, Tabatabaei appears to be silent regarding a source block comprises an adder block as presently claimed. As such, the Examiner is respectfully requested to either (i) (a) provide clear and concise explanation

why one of ordinary skill in the art would consider the BICM of Tabatabaei to be similar to an adder block and (b) explain how the BICM provides with signal Idd or (ii) withdraw the rejection.

Claim 26 provides that the source block comprises a digital source block. Despite the assertion on page 7 of the Office Action, Tabatabaei appears to be silent that the source of the signal Idd (asserted similar to the claimed analog signal) comprises a FF1 (asserted similar to the claimed digital source block). Therefore, the Office Action fails to show anticipation of the claimed structure. As such, claim 26 is fully patentable over the cited reference and the rejection should be withdrawn.

FINALITY OF THE OFFICE ACTION

Applicants' representative respectfully requests reconsideration of the finality of the Office Action. MPEP §706.07 states:

> In making the final rejection, all outstanding ground of rejection of record should be carefully reviewed, and any such grounds relied on in the final rejection should be reiterated. They **must also be clearly developed to such an extent that applicant may readily judge the advisability of an appeal** unless a single previous Office action contains a complete statement supporting the rejection. (Emphasis added)

In contrast, each of the 35 U.S.C. §102 rejections consist of an incomplete sentence that merely points to some paragraph or figure in Tabatabaei. No explanations are provided in the Office Action how the cited text and figures are applied the claim language. As such, none of the 35 U.S.C. §102 rejections have been clearly developed.

IMPROPERLY EXPRESSED REJECTIONS

Applicants' representative respectfully requests that a next Office Action, if any, is a non-final Office Action due to a lack of proper development for the resent rejections. In particular, MPEP §707.07(f) reads:

> Where the applicant traverses any rejection, the examiner should, if he or she repeats the rejection, take note of the applicant's argument and **answer the substance** of it. (Emphasis added)

Applicants' representative traversed the assertion that Tabatabaei anticipates using digital signatures in modeling a design. In contrast, the Office Action only states on page 8 that, "Simulation has been disclosed in section 3 [of Tabatabaei]". The response in the Office Action fails to **answer the substance** of the traverse. No evidence or convincing line of reasoning is provided in the Office Action why Applicants' traverse in incorrect. No cites to particular lines of section 3 of Tabatabaei are provided in the Office Action to show how the claim language is allegedly anticipated. All the Office Action appears to provide is a conclusory statement that somewhere within section 3 of Tabatabaei the claim language is disclosed. Therefore, either a new Office Action or a Notice of Allowance should be issued.

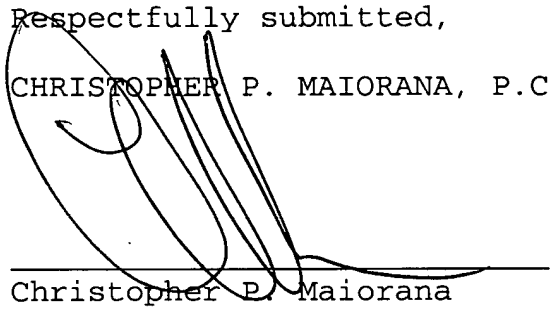
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.



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